STIC Search Report
EIC 2100

STIC Database Tracking Number: 225882

TO: Thanh-ha Dang
Location: RND 3B15
Art Unit: 2163
Thursday, May 24, 2007

Case Serial Number: 10/087360

From: Byron T. Mims
Location: EIC 2100
RND-4B19
Phone: 272-3528

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Search Notes

Thanh-ha

Enclosed are art findings that may be interest, although findings directly relevant did not appear readily apparent. However, I have tagged as well as highlighted the enclosed retrieved items, which seemed most relevant. Let me know if there is anything in particular that you would like for me to pursue further.

Byron

```
Set     Items   Description
S1     398612   DATABASE OR DATABANK OR DATA()(BASE? OR BANK? OR FILE? OR -
             REPOSITOR? OR WAREHOUSE? OR STORE? ? OR STORAG?) OR DB OR RDB
             OR OODB OR ODBC OR DBMS
S2     395441   (TEMPORAR? OR RAM OR VOLITIL?)(3N)(STORE? ? OR STORAG? OR -
             STORING) OR BUFFER? OR CACHE? ? OR CACHING
S3     723352   (UPGRAD? OR REVIS? OR BETTER? OR ENHANC? OR IMPROV? OR AUG-
             MENT? RAIS??? OR INCREAS? OR BOOST?)(5N)(PERFORM? OR EXECUT? -
             OR FUNCTION? OR OPERAT? OR OPTIMI? OR HANDL? OR BEHAV? OR CAP-
             AB?)
S4      22017   (COMPRESS? OR REDUC? OR (CUT OR CUTS OR CUTT? OR DROP? OR -
             LEAV???)(2W)(OUT OR OFF? ?) OR DECREAS? OR DECREMENT? OR PARE?
              OR SHORTEN? OR PARS???)(7N)(BIT OR BITS OR BINARY()DIGIT? ? -
             OR DIGITAL()DATA? ?)
S5      10055   (SHRINK? OR CURTAIL? OR LESSEN? OR LOWER? OR ABRIDG? OR DI-
             SCARD? OR EXCIS? OR DELET? OR (BOX OR BOXES OR BOXED OR BOXIN-
             G)()OUT)(5N)(BIT OR BITS OR BINARY()DIGIT? ? OR DIGITAL()DATA?
              ?)
S6      14012   ((UN OR "NOT" OR IR OR IN)(2N)(RELEVAN? OR WANT??? ? OR NE-
             ED??? ? OR DESIR??? ? OR IMPORTAN?) OR UNDESIR? OR UNWANT? OR
             INSIGNIF? OR UNIMPORTAN?)(5N)(BIT OR BITS OR BINARY()DIGIT? ?
             OR DIGITAL()DATA? ? OR CONTENT? ? OR NUMBER? OR DIGIT? OR CHA-
             RACT?)
S7        842   S6(7N)(DELET? OR REMOV? OR ERADICAT? OR ELIMINAT? OR ERAS?-
             ?? OR EXTRACT? OR (CUT OR CUTS OR CUTT? OR DROP? OR LEAV???)(-
             2W)(OUT OR OFF? ?))
S8       2186   S3 AND S2 AND S1
S9         28   S8 AND (S4:S5 OR S7)
S10         7   S9 AND AC=US/PR AND AY=(2002:2007)/PR
S11        11   S9 AND AC=US AND AY=2002:2007
S12        10   S9 AND AC=US AND AY=(2002:2007)/PR
S13        19   S9 AND PY=2002:2007
S14         7   S8 AND S6
S15         5   S14 NOT S9
S16        26   S8 AND (RECTANG? OR BOX OR BOXE? ? OR BOXING)
S17        23   S16 NOT (S9 OR S14)
S18         4   S17 AND COMPRESS?
S19        19   S17 NOT S18
File 350:Derwent WPIX 1963-2007/UD=200730
        (c) 2007 The Thomson Corporation
File 347:JAPIO Dec 1976-2006/Dec(Updated 070403)
        (c) 2007 JPO & JAPIO
```

13/69,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0016212316 - Drawing available
WPI ACC NO: 2006-743959/ **200676**
XRPX Acc No: N2006-577453
Compressed video data handling method for multiple TV services involves processing data based **on mode of operation selected with respect to source from which compressed video data is received**
Patent Assignee: ATI TECHNOLOGIES INC (ATIT-N)
Inventor: KECHICHIAN K; KOVACEVIC B
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 7113546	B1	20060926	US 2000563211	A	20000502	200676 B

Priority Applications (no., kind, date): US 2000563211 A 20000502

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 7113546	B1	EN	68	51	

Alerting Abstract US B1
NOVELTY - The mode of operation for transmitting and receiving compressed video data at a video **buffer** is selected. The video data received at the transport stream demultiplexer from a head end is processed by the framer and demultiplexer before providing to the video **buffer** , when the initial mode of operation is selected. The data received from the host system is processed after receiving at video **buffer** video processor, when the final mode of operation is selected.
USE - For multiple TV services.
ADVANTAGE - The transport stream information allows more flexibility and **improve performance** in terms of data **handling** , data passing, design implementation, data stream acquisition and standard target decoder (STD) model implementations.
DESCRIPTION OF DRAWINGS - The figure shows the flow chart illustrating compressed video data handling method.

Technology Focus
INDUSTRIAL STANDARDS - The video data is compressed according to ~MPEG-2~ specification.

Title Terms/Index Terms/Additional Words: COMPRESS; VIDEO; DATA; HANDLE; METHOD; MULTIPLE; TELEVISION; SERVICE; PROCESS; BASED; MODE; OPERATE; SELECT; RESPECT; SOURCE; RECEIVE
Class Codes
International Classification (+ Attributes)

IPC + Level	Value	Position	Status	Version
H04N-0011/02	A	I L	B	20060101
H04N-0007/12	A	I F	B	20060101
H04N-0011/00	C	I L	B	20060101

US Classification, Issued: 375240260, 375240020

File Segment: EPI;
DWPI Class: T01; W04
Manual Codes (EPI/S-X): T01-J10D; W04-P01A

Compressed video data handling method for multiple TV services involves processing data based **on mode of operation selected with respect to**

source from which compressed video data is...

Alerting Abstract ...NOVELTY - The mode of operation for transmitting and receiving compressed video data at a video **buffer** is selected. The video data received at the transport stream demultiplexer from a head end is processed by the framer and demultiplexer before providing to the video **buffer** , when the initial mode of operation is selected. The data received from the host system is processed after receiving at video **buffer** video processor, when the final mode of operation is selected....ADVANTAGE - The transport stream information allows more flexibility and **improve performance** in terms of data **handling** , data passing, design implementation, data stream acquisition and standard target decoder (STD) model implementations...

Original Publication Data by Authority

Original Abstracts:
...a plurality of modes for providing and/or receiving compressed video data at a frame **buffer** memory. The modes include providing compressed video data directly from a system host system or...
Claims:
...demultiplexer from a head end;storing the first compressed video data to a compressed video **buffer** associated with a video processor;during a second mode of operation:receiving a second compressed...

...system of the video processor;storing the second compressed video data to the compressed video **buffer** ;during a third mode of operation:receiving a third **compressed** video data having X **bits** from a host bus controller of the host system;storing the third compressed video data in a register;providing the third compressed video **data** **stored** in the register to a framer to provide the third compressed data to the transport ...

...from the transport stream demultiplexer;storing the third compressed video data to a compressed video **buffer** associated with a video processor....
Basic Derwent Week: **200676** ...

13/69,K/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0013647319 - Drawing available
WPI ACC NO: 2003-743280/ **200370**
XRPX Acc No: N2003-595169
Memory e.g. NAND flash memory, has multi-level memory cells accessible through respective word lines and sense lines, and circuit controls application of ascending staircase read signal voltage and read state signals
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: PARKER A
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 6614683	B1	20030902	US 2001794480	A	20010226	200370 B

Priority Applications (no., kind, date): US 2001794480 A 20010226

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 6614683	B1	EN	13	7	

Alerting Abstract US B1
NOVELTY - The memory has multi-level cells accessible through respective word lines and sense lines. A circuit controls application of an ascending staircase read signal voltage to a selected word line and a read state signal to a selected sense line. A switch circuit is responsive to the sense voltage present on a selected sense line, produced in response to the current level present in a bit line of a selected cell.
DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of resolving **data stored** in a memory cell of a multi-level memory capable of storing N stored levels.
USE - Used for storing information.
ADVANTAGE - The multi-level cell devices exponentially increases the storage capacity of a memory device. The ascending staircase read signal applied to the selected word line **reduces** the **bit** line **buffer** circuitry, thereby **reducing** the manufacturing cost of device by 20 to 30 percentage and **improving** the **performance** of the device.
DESCRIPTION OF DRAWINGS - The drawing shows a block diagram of a memory device.
100 memory device
102 Memory cell array

Title Terms/Index Terms/Additional Words: MEMORY; NAND; FLASH; MULTI; LEVEL ; CELL; ACCESS; THROUGH; RESPECTIVE; WORD; LINE; SENSE; CIRCUIT; CONTROL; APPLY; ASCEND; STAIR; READ; SIGNAL; VOLTAGE; STATE

Class Codes
International Classification (Main): G11C-016/04
US Classification, Issued: 365185030, 365185190

File Segment: EPI;
DWPI Class: U14
Manual Codes (EPI/S-X): U14-A03B7; U14-A07A; U14-B01

Alerting Abstract DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of resolving **data stored** in a memory cell of a multi-level memory capable of storing N stored levels...

...of a memory device. The ascending staircase read signal applied to the selected word line **reduces** the **bit** line **buffer** circuitry, thereby **reducing** the manufacturing cost of device by 20 to 30 percentage and **improving** the **performance** of the device...

...

13/69,K/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0013083710 - Drawing available
WPI ACC NO: 2003-164301/ **200316**
Method for compressing multi-dimensional index of main memory database
Patent Assignee: TRANSACT IN MEMORY INC (TRAN-N)
Inventor: CHA S G; KIM G H; KWON G J
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
KR 2002071052	A	20020912	KR 200110780	A	20010302	200316 B

Priority Applications (no., kind, date): KR 200110780 A 20010302

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
KR 2002071052	A	KO	1	10	

Alerting Abstract KR A

NOVELTY - A method for compressing the multi-dimensional index of a main memory **database** is provided to **enhance** the index **cache operation** by reducing a size of the MBR(Minimum Bounding Rectangle) through the quantization of the MBR.

DESCRIPTION - In order to put in more entry into a node, a CR-tree(**Cache** -Conscious R-tree) compresses an MBR key taking 80 percents of the index in case of a two-dimensional index. In order to remove the zero in a front part of the MBR coordinates number, the MBR key is converted into the relative coordinates on the basis of the left lower coordinates of the **parent** MBR. In order to **remove** the **unimportant bits** of the rear part of the relative coordinate number, the quantization is carried out by the fixed bits. Thus, the CR-tree becomes narrower and smaller than an R-tree. The two-dimensional CR-tree represents the similar update performance and the 2.5 times faster search performance than the R-tree while using 60 percents smaller spaces.

Title Terms/Index Terms/Additional Words: METHOD; COMPRESS; MULTI; DIMENSION; INDEX; MAIN; MEMORY; **DATABASE**

Class Codes
International Classification (Main): G06F-012/00

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-H
Method for compressing multi-dimensional index of main memory database

Alerting Abstract ...NOVELTY - A method for compressing the multi-dimensional index of a main memory **database** is provided to **enhance** the index **cache operation** by reducing a size of the MBR(Minimum Bounding Rectangle) through the quantization of the...
DESCRIPTION - In order to put in more entry into a node, a CR-tree(**Cache** -Conscious R-tree) compresses an MBR key taking 80 percents of the index in case...

...converted into the relative coordinates on the basis of the left lower coordinates of the **parent** MBR. In order to **remove** the **unimportant bits** of the rear part of the relative coordinate number, the quantization is carried out by...

Title Terms.../Index Terms/Additional Words: **DATABASE**

...

...

13/69,K/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0013059917 - Drawing available
WPI ACC NO: 2003-139662/ **200313**
XRPX Acc No: N2003-110972
Data processing system has processor which sets dirty and invalidity bits in primary cache **and non-inclusive secondary** cache **in response to writing data lines in primary** cache
Patent Assignee: KOZYRCZAK M P (KOZY-I); NEC ELECTRONICS INC (NIDE); WANG J C (WANG-I)
Inventor: KOZYRCZAK M P; WANG J C
Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 20020174304	A1	20021121	US 2001260100	P	20010105	200313 B
			US 200241932	A	20020107	
US 6715040	B2	20040330	US 200241932	A	20020107	200423 E

Priority Applications (no., kind, date): US 2001260100 P 20010105; US 200241932 A 20020107

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20020174304	A1	EN	14	6	Related to Provisional US 2001260100

Alerting Abstract US A1
NOVELTY - The processor (120) sets a dirty bit and an invalidity bit associated with the data line in a primary **cache** (122) and non-inclusive secondary **cache** in response to non-inclusive secondary **cache** writing the data lines in the primary **cache** .
USE - Data processing system.
ADVANTAGE - **Improves** the **performance** of the data processing system by providing the most recently updated data from the primary **cache** to the processor.
DESCRIPTION OF DRAWINGS - The figure shows the hierarchical structure of memory for the data processing system.
120 Processor
122 Primary **cache**

Title Terms/Index Terms/Additional Words: DATA; PROCESS; SYSTEM; PROCESSOR; SET; DIRT; BIT; PRIMARY; **CACHE** ; NON; INCLUSION; SECONDARY; RESPOND; WRITING; LINE

Class Codes
International Classification (Main): G06F-012/00, G06F-012/12
US Classification, Issued: 711144000, 711136000, 711133000, 711141000, 711159000

File Segment: EPI;
DWPI Class: T01; U14
Manual Codes (EPI/S-X): T01-H01A; T01-H01B3; T01-H03A; U14-A07; U14-A08B

Data processing system has processor which sets dirty and invalidity bits in primary cache **and non-inclusive secondary** cache **in response to writing data lines in primary** cache

Original Titles:
Performance improvement of a write instruction of a non-inclusive

hierarchical **cache** memory unit...

... **Performance improvement** of a write instruction of a non-inclusive hierarchical **cache** memory unit

Alerting Abstract ...a dirty bit and an invalidity bit associated with the data line in a primary **cache** (122) and non-inclusive secondary **cache** in response to non-inclusive secondary **cache** writing the data lines in the primary **cache** . ...ADVANTAGE - **Improves** the **performance** of the data processing system by providing the most recently updated data from the primary **cache** to the processor...

...122 Primary **cache**

Title Terms.../Index Terms/Additional Words: **CACHE** ;

Original Publication Data by Authority

Original Abstracts:
...is a data processing system including a processor, a plurality of caches, and main memory, **the** secondary caches being implemented as **being** non-inclusive, i.e., the lower order caches not storing a **superset** of the data stored in the **next higher** order cache. The non-inclusive **cache** structure provides increased **flexibility** in the storage of data. The operation of a write request operation when the target data line is not found in the primary cache. By using the **dirty** bit associated with each data line, the interaction between the processor and the primary cache can be reduced. **By** using the **invalidity** bit associated with each **data** line, the interaction between the processor and the primary cache can be reduced.
...

...including a processor, a plurality of caches, and main memory, the secondary caches being implemented **as** being non-inclusive, i.e., **the** lower order caches not storing a superset of the data stored **in** the next higher order cache. The **non - inclusive** cache structure provides increased flexibility **in** the storage of **data** . The operation of a write request operation when the target data line is not found in the primary cache. By using the dirty bit associated with each **data** line, the interaction between the processor and the primary cache can be reduced. By using the invalidity bit **associated** with each **data** line, the interaction between **the** processor and the primary cache can be reduced.
Claims:
...cache; anda non-inclusive secondary cache configured to write the data line in the **primary** cache when the primary cache does not **have** the data line;wherein the processor is configured to **set** a dirty bit **associated** with the data line in the primary cache in response to the non-inclusive secondary cache writing the data line in the primary cache, and;wherein **the** processor is configured to set an invalidity **bit** associated with the data line in the **non** -inclusive secondary cache in response to the non-inclusive secondary cache writing the data line in the primary cache.
...

...to a determination that the primary cache lacks memory space to store another data line; **selecting** an unmodified data line in one of a plurality of secondary caches;overwriting the unmodified data **line** in the one of the plurality secondary caches with **a** copy of the victim line selected in the primary cache;overwriting the victim data line in the primary cache

with a copy **of** the first data line contained in the one or another of the plurality of **secondary** caches;setting a dirty bit associated with the first data line **in** the primary cache after the victim data line in the **primary** cache is overwritten with the copy of the first data line;setting an invalid bit associated with the first **data** line contained in the one or another of the plurality of secondary caches. ...
Basic Derwent Week: **200313** ...

13/69,K/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0012773649 - Drawing available
WPI ACC NO: 2002-627947/ **200267**
XRPX Acc No: N2002-496521
Improving **method for** cache behaviour **of accessing multidimensional index structure resident in main memory for facilitating reference to data objects stored in a** database
Patent Assignee: CHA S K (CHAS-I); KIM K (KIMK-I); KWON K (KWON-I); TRANSACT IN MEMORY INC (TRAN-N)
Inventor: CHA S K; KIM K; KIM K H; KWON K; KWON K J
Patent Family (6 patents, 98 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
WO 2002071270	A1	20020912	WO 2002KR378	A	20020305	200267	B
US 20020169784	A1	20021114	US 2001272828	P	20010305	200277	E
			US 200287360	A	20020301		
EP 1366437	A1	20031203	EP 2002705525	A	20020305	200380	E
			WO 2002KR378	A	20020305		
CN 1462399	A	20031217	CN 2002801435	A	20020305	200420	E
AU 2002239086	A1	20020919	AU 2002239086	A	20020305	200433	E
JP 2004519774	W	20040702	JP 2002570125	A	20020305	200443	E
			WO 2002KR378	A	20020305		

Priority Applications (no., kind, date): US 200287360 A 20020301; US 2001272828 P 20010305

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
WO 2002071270	A1	EN	54	21	

National Designated States,Original: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
Regional Designated States,Original: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

US 20020169784	A1	EN		Related to Provisional US 2001272828
EP 1366437	A1	EN		PCT Application WO 2002KR378
				Based on OPI patent WO 2002071270

Regional Designated States,Original: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

AU 2002239086	A1	EN		Based on OPI patent WO 2002071270
JP 2004519774	W	JA	96	PCT Application WO 2002KR378
				Based on OPI patent WO 2002071270

Alerting Abstract WO A1

NOVELTY - The method involves associating with each node a minimum bounding rectangle (MBR). Each MBR is the minimal hyper-rectangle enclosing the corresponding data object in the case of a leaf node and all the hyper-rectangles in the child node in the case of an internal node.

Each of one or more MBRs is represented by a relative representation of a MBR (RMBR) that is the co-ordinates of the MBR represented relative to the co-ordinates of a reference MBR. Each RMBR is compressed into a quantized RMBR (QRMBR) by quantizing each RMBR to finite precision by **cutting off** training **insignificant bits** after quantization.

DESCRIPTION - INDEPENDENT CLAIMS are included for a multidimensional index structure and for an index tree.

USE - For **database** systems.
ADVANTAGE - **Improves** index **cache** **behaviour** in main-memory **database** systems.
DESCRIPTION OF DRAWINGS - The figure shows the QRMBR technique of the invention.

Title Terms/Index Terms/Additional Words: IMPROVE; METHOD; **CACHE** ; BEHAVE; ACCESS; MULTIDIMENSIONAL; INDEX; STRUCTURE; RESIDENCE; MAIN; MEMORY; FACILITATE; REFERENCE; DATA; OBJECT; STORAGE; **DATABASE**

Class Codes
International Classification (Main): G06F-012/00, G06F-017/30, G06F-007/00
US Classification, Issued: 707102000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-H03A; T01-J05B1; T01-J05B3; T01-J05B4C

Improving **method for** cache behaviour **of accessing multidimensional index structure resident in main memory for facilitating reference to data objects stored in a** database

Original Titles:
KOMPRESSIONSSCHEMA ZUR VERBESSERUNG DES **CACHE** -VERHALTENS IN DATENBANKSYSTEMEN...

...COMPRESSION SCHEME FOR **IMPROVING** **CACHE** **BEHAVIOR** IN **DATABASE** SYSTEMS...

...PROGRAMME DE COMPRESSION PERMETTANT D'AMELIORER LE COMPORTEMENT DU **CACHE** DANS LES SYSTEMES DE BASES DE DONNEES...
...Compression scheme for **improving** **cache** **behavior**
...

...COMPRESSION SCHEME FOR **IMPROVING** **CACHE** **BEHAVIOR** IN **DATABASE** SYSTEMS...

...PROGRAMME DE COMPRESSION PERMETTANT D'AMELIORER LE COMPORTEMENT DU **CACHE** DANS LES SYSTEMES DE BASES DE DONNEES

Alerting Abstract ...is compressed into a quantized RMBR (QRMBR) by quantizing each RMBR to finite precision by **cutting** **off** training **insignificant** **bits** after quantization....USE - For **database** systems...

...ADVANTAGE - **Improves** index **cache** **behaviour** in main-memory **database** systems...

Title Terms.../Index Terms/Additional Words: **CACHE** ; ...

... **DATABASE**

Original Publication Data by Authority

Original Abstracts:
A cache-conscious version of **the** R-tree, called the CR-tree, is disclosed. To pack more entries in a node...

...Then, it quantizes the relative coordinates with a fixed number of bits to further cut **off** the trailing **less** **significant** bits. Consequently,

the CR- **tree** becomes significantly wider and smaller than the ordinary R-tree. The experimental and analytical results...

...A cache-conscious version of the R-tree, called the **CR** -tree, is disclosed. To pack more entries in a node, the CR-tree compresses MBR...

...coordinates with a fixed number of bits to further cut off the trailing less significant **bits** . Consequently, the **CR - tree** becomes significantly wider and **smaller** than the ordinary R-tree. The experimental and analytical results show that the two-dimensional...

...A cache-conscious version of the R-tree, called the CR-tree, is disclosed. To **pack** more entries in a node, the CR-tree compresses MBR keys, which occupy substantial part...

...of bits to further cut off the trailing less significant bits. Consequently, the CR-tree **becomes** significantly wider **and** **smaller** than the ordinary R- **tree** . The experimental and analytical results show that the two-dimensional CR-tree performs search faster...

...R appelee arbre CR. Afin de regrouper davantage d'entrees dans un noeud, l'arbre **CR** comprime les cles MBR qui occupent une partie substantielle des donnees d'index. Cet arbre...

Claims:

...claimed is: 1. A method of improving the cache behavior of accessing a multidimensional index **structure** resident **in** **main** memory for facilitating reference to data objects stored in a database, where the index structure consists of internal nodes **having** pointers to child nodes and leaf nodes having to database objects, the method comprising the steps of: associating **with** each node a minimum bounding rectangle ("MBR"), wherein each MBR is the minimal hyper-rectangle ...

...

13/69,K/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0009657979 - Drawing available
WPI ACC NO: 1999-610907/199952
XRPX Acc No: N1999-450156
Data storage **controller for AMPIC-DRAM management system**
Patent Assignee: NEXABIT NETWORKS INC (NEXA-N); NEXABIT NETWORKS LLC (LUCE)
Inventor: PAL S; SOMAN S S
Patent Family (8 patents, 81 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
WO 1999051000	A1	19991007	WO 1999IB482	A	19990322	199952	B
AU 199932703	A	19991018	AU 199932703	A	19990322	200010	E
US 6138219	A	20001024	US 199849567	A	19980327	200055	E
EP 1070408	A1	20010124	EP 1999941293	A	19990322	200107	E
			WO 1999IB482	A	19990322		
CN 1298593	A	20010606	CN 1999805498	A	19990322	200157	E
TW 435028	A	20010516	TW 1999104830	A	19990714	200170	E
JP 2002510813	W	20020409	WO 1999IB482	A	19990322	200227	E
			JP 2000541803	A	19990322		
AU 748504	B	20020606	AU 199932703	A	19990322	200249	E

Priority Applications (no., kind, date): US 199849567 A 19980327

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
WO 1999051000	A1	EN	36	9	
National Designated States,Original: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW					
Regional Designated States,Original: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ UG ZW					
AU 199932703	A	EN			Based on OPI patent WO 1999051000
EP 1070408	A1	EN			PCT Application WO 1999IB482
					Based on OPI patent WO 1999051000
Regional Designated States,Original: DE FR GB IT SE					
TW 435028	A	ZH			
JP 2002510813	W	JA	40		PCT Application WO 1999IB482
					Based on OPI patent WO 1999051000
AU 748504	B	EN			Previously issued patent AU 9932703
					Based on OPI patent WO 1999051000

Alerting Abstract WO A1

NOVELTY - **Buffered** asynchronous transfer mode (ATM) data corresponding to each memory bank from input data read resource ports is stored in the DRAM containing array of internally **cached** (AMPIC) banks. The storage of specific cell in the slot **buffer** of DRAM is regulated by cross-bar switches connected between input write port and slot **buffer** .

DESCRIPTION - The header destination data corresponding to input read resource port is forwarded to the slot **buffer** . The **buffer** is divided into several cells corresponding to the number of system input resources, such that each **buffer** stores 64 bytes data. The write resource ports correspond to various DRAM banks while the read resource ports corresponds to specific banks. An INDEPENDENT CLAIM is also included for the **data storage** control method.

USE - For AMPIC-DRAM management in ATM, wavelength division multiplexing (WDM) based communication system, synchronous optical network (SONET).

ADVANTAGE - Enables storage of data from various input resources in single or multiple slots, and hence raises storage capacity. Reduces bus contention of DRAM, by effective utilization of **buffer** slots.
DESCRIPTION OF DRAWINGS - The figure shows the block diagram of the AMPIC-DRAM management system.

Title Terms/Index Terms/Additional Words: DATA; STORAGE; CONTROL; DRAM; MANAGEMENT; SYSTEM

Class Codes
International Classification (Main): G06F-012/06, G06F-013/14, H04L-012/56
(Additional/Secondary): G06F-012/00, H04L-012/28
US Classification, Issued: 711149000, 711119000, 711105000

File Segment: EPI;
DWPI Class: W01; W02
Manual Codes (EPI/S-X): W01-A03B1; W01-A06C1; W01-A06E1; W01-A06F; W01-A06G2; W01-B07; W02-C04B4B

Data storage **controller for AMPIC-DRAM management system**

Original Titles:
...Method of and **operating** architectural **enhancement** for multi-port internally **cached** dynamic random access memory (AMPIC DRAM) systems, eliminating external control paths and random memory addressing...

Alerting Abstract ...NOVELTY - **Buffered** asynchronous transfer mode (ATM) data corresponding to each memory bank from input data read resource ports is stored in the DRAM containing array of internally **cached** (AMPIC) banks. The storage of specific cell in the slot **buffer** of DRAM is regulated by cross-bar switches connected between input write port and slot **buffer** . ...The header destination data corresponding to input read resource port is forwarded to the slot **buffer** . The **buffer** is divided into several cells corresponding to the number of system input resources, such that each **buffer** stores 64 bytes data. The write resource ports correspond to various DRAM banks while the read resource ports corresponds to specific banks. An INDEPENDENT CLAIM is also included for the **data storage** control method...

...slots, and hence raises storage capacity. Reduces bus contention of DRAM, by effective utilization of **buffer** slots...

Original Publication Data by Authority

Original Abstracts:
...technique and system for eliminating bus contention in multi-port internally cached dynamic random access **memory** (AMPIC DRAM) systems, while eliminating the need for external control paths and random memory addressing, through the use of data header destination bits and a novel **dedication** of reduced size slot buffers **to** separate DRAM **banks** and similarly dedicated I/O data read resource ports, particularly useful for relatively short ATM...

...enabled simultaneously to write complete ATM messages into a single slot buffer, and also for **SONET** Cross Connect and WDM messages...

...and system for eliminating bus contention in multi-port internally cached dynamic random access memory (**AMPIC** DRAM) systems, while eliminating the need for external control paths and random memory

addressing, through the use of data header destination bits and a novel dedication **of** reduced size slot buffers to **separate** DRAM banks **and** similarly dedicated I/O data read resource ports, particularly useful for relatively short ATM message...

...simultaneously to write complete ATM messages into a single slot buffer, and also for SONET **Cross** Connect and WDM messages...

...bus contention in multi-port internally cached dynamic random access memory (AMPIC DRAM) systems, while **eliminating** the need for external control paths and random memory addressing, through the use of data header destination bits and a novel dedication of reduced size slot **buffers** to separate DRAM banks and **similarly** dedicated I/ **O** data read resource ports, particularly useful for relatively short ATM message networking and the like...

...ATM messages into a single slot buffer, and also for SONET Cross Connect and WDM **messages** .

Claims:
...an improved DRAM architecture comprisingan array of multi-port internally cached DRAM banks (AMPIC **DRAM**) each comprising a plurality of independent serial data interfaces connected between a separate external I ...
...port and the corresponding internal DRAM memory through a corresponding data caching multi-cell slot **buffer** ;each DRAM bank **being** connected to a single multi-cell slot buffer and to a single destination **I** /O data read resource port, each multi-cell slot buffer dedicated to that DRAM bank **for** respectively storing buffered data destined for that DRAM **bank** and for reading out the stored data solely to the dedicated I/O data read...

...write resource port and the corresponding slot buffer, but with all I/O data write **resource** ports connected to input data to each cross-bar switch, allowing the I/O data

13/69,K/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0009097443 - Drawing available
WPI ACC NO: 1999-016532/199902
XRPX Acc No: N1999-013295
MPEG image editor - compares amounts of data stored **in virtual** buffer **of first and second node based on which number of bits in third bit stream interlinking first and second bit stream is regulated**
Patent Assignee: SONY CORP (SONY)
Inventor: ANDO Y; ANTO H; HIROJI A
Patent Family (6 patents, 4 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
JP 10285529	A	19981023	JP 199786251	A	19970404	199902	B
CN 1195949	A	19981014	CN 1998106237	A	19980406	199909	E
KR 1998081098	A	19981125	KR 199811980	A	19980404	200005	E
US 6137946	A	20001024	US 199854858	A	19980403	200055	E
CN 1192609	C	20050309	CN 1998106237	A	19980406	200634	E
KR 563183	B1	20060725	KR 199811980	A	19980404	200728	E

Priority Applications (no., kind, date): JP 199786251 A 19970404

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
JP 10285529	A	JA	24	16	
KR 1998081098	A	KO		17	
KR 563183	B1	KO		16	Previously issued patent KR 9881098

Alerting Abstract JP A
The image editor edits first and second **bit** stream which are obtained by performing **compression** encoding of an image. A third **bit** stream is provided that interlinks with the above **bit** streams. The **compression** encoding is performed with respect to capacity of virtual **buffer** of first node and the encoded data is stored in the first node.
A second node is connected to the first node. A calculator (24) calculates the capacity of **buffer** of second node. Based on the capacity difference between the two virtual **buffers** , the data bits in the third bit stream is regulated.
ADVANTAGE - **Enhances** to **perform** editing at high speed.

Title Terms/Index Terms/Additional Words: IMAGE; EDIT; COMPARE; AMOUNT; DATA; STORAGE; VIRTUAL; **BUFFER** ; FIRST; SECOND; NODE; BASED; NUMBER; BIT ; THIRD; STREAM; INTERLINKED; REGULATE

Class Codes
International Classification (Main): H04N-005/76
International Classification (+ Attributes)

IPC + Level	Value	Position	Status	Version
G11B-0027/02	A	I L	R	20060101
G11B-0027/031	A	I L	R	20060101
G11B-0027/034	A	I	R	20060101
H04N-0005/765	A	I	R	20060101
H04N-0005/77	A	N	R	20060101
H04N-0005/775	A	N	R	20060101
H04N-0005/91	A	I F	R	20060101
H04N-0005/92	A	I L	R	20060101
H04N-0007/24	A	I	R	20060101
G11B-0027/02	A	I F	B	20060101

H04N-0005/76 A I F B 20060101
G11B-0027/02 C I L R 20060101
G11B-0027/031 C I R 20060101
H04N-0005/765 C I R 20060101
H04N-0005/77 C N R 20060101
H04N-0005/775 C N R 20060101
H04N-0005/91 C I F R 20060101
H04N-0005/92 C I L R 20060101
H04N-0007/24 C I R 20060101
G11B-0027/02 C I F B 20060101
H04N-0005/76 C I F B 20060101
US Classification, Issued: 386111000, 386052000

File Segment: EPI;
DWPI Class: W04
Manual Codes (EPI/S-X): W04-F; W04-F01; W04-H05

...**compares amounts of** data stored **in virtual** buffer **of first and second node based on which number of bits in third bit stream**...

Original Titles:
...Picture editing apparatus and method using virtual **buffer** estimation.

Alerting Abstract ...The image editor edits first and second **bit** stream which are obtained by performing **compression** encoding of an image. A third **bit** stream is provided that interlinks with the above **bit** streams. The **compression** encoding is performed with respect to capacity of virtual **buffer** of first node and the encoded data is stored in the first node...

...second node is connected to the first node. A calculator (24) calculates the capacity of **buffer** of second node. Based on the capacity difference between the two virtual **buffers** , the data bits in the third bit stream is regulated...

...ADVANTAGE - **Enhances** to **perform** editing at high speed.

Title Terms.../Index Terms/Additional Words: **BUFFER** ;

Original Publication Data by Authority

Original Abstracts:
...Aout of a scene Aprime of the bit stream A and the amount of data **DB** at a start point Bin of a scene Bprime of the bit stream B to be accumulated in a VBV **buffer** are calculated. The difference between DA and **DB** is used for adjusting the amount of data at a portion of the bit stream...

...corresponds to a point of junction between the bit streams A and B. If DA> **DB** , stuffing code is added to a picture at the end point Aout. If DA< **DB** , on the other hand, skipped P pictures are inserted into a location after the picture...
Claims:
...portion of a second bit stream also obtained as a result of said operation to **compress** and encode pictures, thereby composing a third **bit** stream through editing said first and second **bit** streams, wherein said operation to **compress** and encode pictures is carried out by considering an amount of data to be accumulated in a virtual **buffer** on a receiving side, and wherein accumulation quantity information on said amount of data to...

...quantity computing means for computing an amount of data to be accumulated in said virtual **buffer** at a first point of junction on said first bit stream for connecting said first...

...bit stream and for computing an amount of data to be accumulated in said virtual **buffer** at a second point of junction on said second bit stream for connecting said second...

...accordance with a difference between said amounts of data to be accumulated in said virtual **buffer** at said first and second points of junction computed by said data accumulation quantity computing...

...MPEG (Moving Picture Expert Group) specifications, wherein said accumulation quantity information is a VD (Video **Buffering** Verifier Delay) which is included in a picture header and corresponds to said amount of data to be accumulated, wherein said virtual **buffer** is a VBV (Video **Buffering** Verifier) **buffer** , and wherein said data quantity adjusting means inserts data of a skipped P picture to...

...first point of junction if said amount of data to be accumulated in said VBV **buffer** at said first point of junction is smaller than said amount of data to be accumulated in said VBV **buffer** at said second point of junction.

13/69,K/15 (Item 15 from file: 350)

0008740093 - Drawing available
WPI ACC NO: 1998-282079/199825
Related WPI Acc No: 2007-275369
XRPX Acc No: N1998-222613

Condensed data memory device for camera - has system controller that detects condition of disc unit by which recording of compressed data is impossible, and enlarges compressing rate of compressing circuit if such condition exist

Patent Assignee: SHARP KK (SHAF)
Inventor: AKIYAMA A; AKIYAMA J

Patent Family (3 patents, 2 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
JP 10097764	A	19980414	JP 1997139587	A	19970529	199825	B
US 6065094	A	20000516	US 1997900173	A	19970725	200031	E
JP 3859815	B2	20061220	JP 1997139587	A	19970529	200701	E

Priority Applications (no., kind, date): JP 1996204446 A 19960802; JP 1997139587 A 19970529

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
JP 10097764	A	JA	13	8	
JP 3859815	B2	JA	17		Previously issued patent JP 10097764

Alerting Abstract JP A

The device has a **compressing** circuit (1) that **compresses** the **digital data** coming from a camera unit (8). The resulting compressed data are **temporarily stored** into a **buffer** memory (2). A disc unit (4) stores the compressed data at a rate faster than that used in storing compressed into **buffer** memory.

The condition by which recording of compressed data into the disc unit becomes impossible is detected by a system controller (5). If such a condition is detected, the controller enlarges the compression rate of the compressing circuit.

ADVANTAGE - Capacity of **buffer** memory can be made small by increasing data compressing rate, thus **improving** earthquake-resisting **capability** of device. Low cost. Reduces number of data that should be compressed. Ensures effective correspondence between device and user.

Title Terms/Index Terms/Additional Words: CONDENSATION; DATA; MEMORY; DEVICE; CAMERA; SYSTEM; CONTROL; DETECT; CONDITION; DISC; UNIT; RECORD; COMPRESS; IMPOSSIBLE; ENLARGE; RATE; CIRCUIT; EXIST

Class Codes

International Classification (Main): G11B-020/10
International Classification (+ Attributes)

IPC + Level	Value	Position	Status	Version
G11B-0020/00	A	N	R	20060101
G11B-0020/10	A	I F	B	20060101
G11B-0020/10	A	I	R	20060101
G11B-0020/00	C	N	R	20060101
G11B-0020/10	C	I F	B	20060101
G11B-0020/10	C	I	R	20060101

US Classification, Issued: 710052000, 710057000, 710060000, 710068000,

711111000, 711112000

File Segment: EPI;
DWPI Class: W04
Manual Codes (EPI/S-X): W04-C10A3; W04-M01D9; W04-P01A

Original Titles:
...Inexpensive compressed **data storage** apparatus with improved resistance to vibrations.

Alerting Abstract ...The device has a **compressing** circuit (1) that **compresses** the **digital data** coming from a camera unit (8). The resulting compressed data are **temporarily stored** into a **buffer** memory (2). A disc unit (4) stores the compressed data at a rate faster than that used in storing compressed into **buffer** memory...

...ADVANTAGE - Capacity of **buffer** memory can be made small by increasing data compressing rate, thus **improving** earthquake-resisting **capability** of device. Low cost. Reduces number of data that should be compressed. Ensures effective correspondence...

Original Publication Data by Authority

Original Abstracts:
A compressed **data storage** apparatus is provided with a **compressing** circuit for generating **compressed** data by **compressing digital data** from a camera section, a **buffer** memory for **storing** the compressed data **temporarily** , a disk device for storing the compressed **data stored** in the **buffer** memory at a rate faster than a rate at which the **buffer** memory stores the compressed data, and a system controller for increasing a compression ratio of...

...or an impact, the data compression ratio is increased, whereby the rate at which the **buffer** memory stores the data is reduced. Consequently, the capacity of the **buffer** memory can be reduced, and therefore, it has become possible to provide an inexpensive compressed **data storage** apparatus with excellent resistance to vibrations.
Claims:
A compressed **data storage** apparatus for storing data after compressing the data, comprising:compressing means for generating compressed data by compressing the data; **temporary storage** means for **temporarily storing** the compressed **data** ; **storage** means for storing the compressed data by retrieving the compressed data from said **temporary storage** means at a rate faster than an output rate at which said compressing means outputs the compressed data to said **temporary storage** means; andcontrol means for, when detecting that said storage means has become unable to...

13/69,K/19 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0005967738 - Drawing available
WPI ACC NO: 1992-200468/199224
XRPX Acc No: N1992-151614
Electronic still video camera with PC compatible format output - uses compression algorithm with digital picture signals and operator control of format compatibility
Patent Assignee: CHIKOSKY M A (CHIK-I); PERSONAL COMPUTER CAMERAS INC (PERS-N); ROBERTS M K (ROBE-I); SPEASL J A (SPEA-I); ST CLAIR INTELLECTUAL PROPERTY CONSULTAN (SCLA-N); ST CLAIR INTELLECTUAL PROPERTY CONSULTANTS INC (SCLA-N)
Inventor: CHIKOSKY M A; ROBERTS M K; SPEASL J A
Patent Family (22 patents, 33 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
WO 1992009169	A1	19920529	WO 1991US8500	A	19911120	199224	B
US 5138459	A	19920811	US 1990615848	A	19901120	199235	E
AU 199191422	A	19920611	AU 199191422	A	19911120	199237	E
			WO 1991US8500	A	19911120		
EP 558670	A1	19930908	WO 1991US8500	A	19911120	199336	E
			EP 1992902180	A	19911120		
JP 6505841	W	19940630	WO 1991US8500	A	19911120	199430	E
			JP 1992502638	A	19911120		
EP 558670	A4	19931013	WO 1991CH222	A	19911030	199527	E
US 5576757	A	19961119	US 1990615848	A	19901120	199701	E
			US 1992878603	A	19920505		
			US 199398787	A	19930729		
EP 558670	B1	19990414	WO 1991US8500	A	19911120	199919	E
			EP 1992902180	A	19911120		
DE 69131138	E	19990520	DE 69131138	A	19911120	199926	E
			WO 1991US8500	A	19911120		
			EP 1992902180	A	19911120		
US 6094219	A	20000725	US 1990615848	A	19901120	200038	E
			US 1992878603	A	19920505		
			US 199398787	A	19930729		
			US 1996651562	A	19960522		
KR 222359	B1	19991001	WO 1991US8500	A	19911120	200108	E
			KR 1993701490	A	19930519		
US 6233010	B1	20010515	US 1990615848	A	19901120	200129	E
			US 1992878603	A	19920505		
			US 199398787	A	19930729		
			US 1996712493	A	19960911		
			US 1999253831	A	19990219		
US 6323899	B1	20011127	US 1990615848	A	19901120	200175	E
			US 1992878603	A	19920505		
			US 199398787	A	19930729		
			US 1996651562	A	19960522		
			US 2000541285	A	20000403		
CA 2095817	C	20020101	CA 2095817	A	19911120	200212	E
			WO 1991US8500	A	19911120		
JP 2002325194	A	20021108	JP 1992502638	A	19911120	200305	E
			JP 200267371	A	19911120		
US 6496222	B1	20021217	US 1990615848	A	19901120	200307	E
			US 1992878603	A	19920505		
			US 199398787	A	19930729		
			US 1996712493	A	19960911		
			US 1999253831	A	19990219		
			US 2000724375	A	20001127		

US 20030025807	A1	20030206	US 1990615848	A	19901120	200313	E
			US 1992878603	A	19920505		
			US 199398787	A	19930729		
			US 1996712493	A	19960911		
			US 1999253831	A	19990219		
			US 2000724375	A	20001127		
			US 2002241886	A	20020912		
JP 2004222314	A	20040805	JP 200267371	A	19911120	200451	E
			JP 200462416	A	20040305		
JP 3741656	B2	20060201	JP 1992502638	A	19911120	200613	E
			JP 200267371	A	20020312		
US 6323899	C1	20061128	US 1990615848	A	19901120	200680	E
			US 1992878603	A	19920505		
			US 199398787	A	19930729		
			US 1996651562	A	19960522		
			US 2000541285	A	20000403		
US 6094219	C1	20061219	US 1990615848	A	19901120	200704	E
			US 1992878603	A	19920505		
			US 199398787	A	19930729		
			US 1996651562	A	19960522		
US 6233010	C1	20070227	US 1990615848	A	19901120	200718	E
			US 1992878603	A	19920505		
			US 199398787	A	19930729		
			US 1996712493	A	19960911		
			US 1999253831	A	19990219		

Priority Applications (no., kind, date): US 1990615848 A 19901120; US 1992878603 A 19920505; US 199398787 A 19930729; US 1996651562 A 19960522; US 1996712493 A 19960911; US 1999253831 A 19990219; US 2000541285 A 20000403; US 2000724375 A 20001127; US 2002241886 A 20020912

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
WO 1992009169	A1	EN	37	14	
National Designated States,Original: AU BB BG BR CA FI HU JP KP KR LK MC MG MW NO PL RO SD SU					
Regional Designated States,Original: AT BE CH DE DK ES FR GB GR IT LU NL SE					
US 5138459	A	EN	20		
AU 199191422	A	EN			PCT Application WO 1991US8500 Based on OPI patent WO 1992009169
EP 558670	A1	EN	37	14	PCT Application WO 1991US8500 Based on OPI patent WO 1992009169
Regional Designated States,Original: DE GB					
JP 6505841	W	JA	15	1	PCT Application WO 1991US8500 Based on OPI patent WO 1992009169
EP 558670	A4	EN			
US 5576757	A	EN	20	14	Continuation of application US 1990615848 Continuation of application US 1992878603 Continuation of patent US 5138459
EP 558670	B1	EN			PCT Application WO 1991US8500 Based on OPI patent WO 1992009169
Regional Designated States,Original: DE GB					
DE 69131138	E	DE			PCT Application WO 1991US8500 Application EP 1992902180 Based on OPI patent EP 558670 Based on OPI patent WO 1992009169
US 6094219	A	EN			Continuation of application US

1990615848				
				Continuation of application US
1992878603				
				Continuation of application US
199398787				
				Continuation of patent US 5138459
				Continuation of patent US 5576757
KR 222359	B1	KO		PCT Application WO 1991US8500
US 6233010	B1	EN		Continuation of application US
1990615848				
				Continuation of application US
1992878603				
				Continuation of application US
199398787				
				Continuation of application US
1996712493				
				Continuation of patent US 5138459
				Continuation of patent US 5576757
US 6323899	B1	EN		Continuation of application US
1990615848				
				Continuation of application US
1992878603				
				Continuation of application US
199398787				
				Continuation of application US
1996651562				
				Continuation of patent US 5138459
				Continuation of patent US 5576757
				Continuation of patent US 6094219
CA 2095817	C	EN		PCT Application WO 1991US8500
				Based on OPI patent WO 1992009169
JP 2002325194	A	JA	15	Division of application JP 1992502638
US 6496222	B1	EN		Continuation of application US
1990615848				
				Continuation of application US
1992878603				
				Continuation of application US
199398787				
				Continuation of application US
1996712493				
				Continuation of application US
1999253831				
				Continuation of patent US 5138459
				Continuation of patent US 5576757
				Continuation of patent US 6233010
US 20030025807	A1	EN		Continuation of application US
1990615848				
				Continuation of application US
1992878603				
				Continuation of application US
199398787				
				Continuation of application US
1996712493				
				Continuation of application US
1999253831				
				Continuation of application US
2000724375				
				Continuation of patent US 5138459
				Continuation of patent US 5576757
				Continuation of patent US 6233010

				Continuation of patent US 6496222
JP 2004222314	A	JA	20	Division of application JP 200267371
JP 3741656	B2	JA	18	Division of application JP 1992502638
				Previously issued patent JP 2002325194
US 6323899	C1	EN		Continuation of application US 1990615848
				Continuation of application US 1992878603
				Continuation of application US 199398787
				Continuation of application US 1996651562
				Continuation of patent US 5138459
				Continuation of patent US 5576757
				Continuation of patent US 6094219
US 6094219	C1	EN		Continuation of application US 1990615848
				Continuation of application US 1992878603
				Continuation of application US 199398787
				Continuation of patent US 5138459
				Continuation of patent US 5576757
US 6233010	C1	EN		Continuation of application US 1990615848
				Continuation of application US 1992878603
				Continuation of application US 199398787
				Continuation of application US 1996712493
				Continuation of patent US 5138459
				Continuation of patent US 5576757

Alerting Abstract WO A1

The camera has a shutter mechanism associated with a lens, an array of discrete light sensing pixels elements and a focus and range central circuit. A pixel multiplexing circuit separates an output from each pixel element into its primary colour components. An A/D converter changes the analog signals into corresponding digital signals.

A **digital data compression** algorithm is applied to the digital signals to generate compressed information signals. There are operator selectable controls for controlling **digital data** format compatibility between the **compressed** signals, and one of a number of operator selectable types of computer apparatus.

ADVANTAGE - Provides digital image files for immediate and direct incorporation into popular word processing, desktop publishing, and other software programs on PCs.

Equivalent Alerting Abstract US A

The camera comprises a lens, shutter, and exposure control system, a focus and range control circuit and a solid state imaging device incorporating a Charge Couple Device (CCD) through which an image is focused. A digital control unit which times control of an image for electronic processing is accomplished and an Analog-to-Digital (A/D) converter circuit converts the analog picture signals into their digital equivalents.

A pixel **buffer** collects a complete row of an image's digital

equivalent. A selectively adjustable digital image compression and decompression algorithm compresses the size of a digital image and selectively formats the compressed digital image to a compatible format for either the IBM Personal Computer and related architectures or the Apple Macintosh PC architecture as selected by the operator so that the digital image can be directly read into most word processing, desktop publishing.

ADVANTAGE - Provides an **improved** electronic still camera with **operator** selectable picture compression in one of a number of operator selectable digital data formats recordable on a standard removable magnetic discette common to personal computers.

Title Terms/Index Terms/Additional Words: ELECTRONIC; STILL; VIDEO; CAMERA; COMPATIBLE; FORMAT; OUTPUT; COMPRESS; ALGORITHM; DIGITAL; PICTURE; SIGNAL ; OPERATE; CONTROL

Class Codes

International Classification (Main): H04N-005/225, H04N-005/30
(Additional/Secondary): G11B-031/00, H04N-001/00, H04N-001/21, H04N-005/232, H04N-005/781, H04N-005/91

International Classification (+ Attributes)

IPC + Level Value	Position	Status	Version
G11B-0031/00 A	I F	R	20060101
H04N-0001/00 A	I	R	20060101
H04N-0001/21 A	I	R	20060101
H04N-0101/00 A	N L	R	20060101
H04N-0101/00 A	N L	B	20060101
H04N-0005/225 A	I	R	20060101
H04N-0005/225 A	I L	R	20060101
H04N-0005/225 A	I F	B	20060101
H04N-0005/225 A	I F		20060101
H04N-0005/232 A	I L	R	20060101
H04N-0005/30 A	I	R	20060101
H04N-0005/76 A	I	R	20060101
H04N-0005/765 A	I L	R	20060101
H04N-0005/781 A	I L	R	20060101
H04N-0005/91 A	I L	R	20060101
H04N-0005/92 A	I L	R	20060101
H04N-0007/01 A	I	R	20060101
H04N-0007/26 A	I	R	20060101
H04N-0005/262 A	I L		20060101
G11B-0031/00 C	I F	R	20060101
H04N-0001/00 C	I	R	20060101
H04N-0001/21 C	I	R	20060101
H04N-0005/225 C	I	R	20060101
H04N-0005/225 C	I L	R	20060101
H04N-0005/225 C	I L	B	20060101
H04N-0005/232 C	I L	R	20060101
H04N-0005/30 C	I	R	20060101
H04N-0005/76 C	I	R	20060101
H04N-0005/765 C	I L	R	20060101
H04N-0005/781 C	I L	R	20060101
H04N-0005/91 C	I L	R	20060101
H04N-0005/92 C	I L	R	20060101
H04N-0007/01 C	I	R	20060101
H04N-0007/26 C	I	R	20060101
H04N-0005/225 C	I		20060101
H04N-0005/262 C	I		20060101

US Classification, Issued: 348231900, 348231700, 358093000, 358140000, 358903000, 358209000, 348220000, 348232000, 358906000, 348207000, 348220000, 348552000, 348207000, 348207000, 348220000, 348231000, 348207000, 348220000, 348220000, 348207000, 348231000

File Segment: EPI;
DWPI Class: T01; W04
Manual Codes (EPI/S-X): T01-C; T01-D02; W04-B14; W04-F01F; W04-K; W04-M01B1A

Alerting Abstract ...A **digital data compression** algorithm is applied to the digital signals to generate compressed information signals. There are operator selectable controls for controlling **digital data** format compatibility between the **compressed** signals, and one of a number of operator selectable types of computer apparatus...

Equivalent Alerting Abstract ...A pixel **buffer** collects a complete row of an image's digital equivalent. A selectively adjustable digital image...

...ADVANTAGE - Provides an **improved** electronic still camera with **operator** selectable picture compression in one of a number of operator selectable digital data formats recordable...

Original Publication Data by Authority

Original Abstracts:
...converter circuit (8) to convert the analog picture signals into their digital equivalents, a pixel **buffer** (10) for collecting a complete row of an image's digital equivalent, a frame **buffer** (11) for collecting all rows of an image's digital equivalent,and a selectively adjustable...

...that the digital image can be directly read into most word processing, desktop publishing, and **data base** software packages...

...D) converter circuit to convert the analog picture signals into their digital equivalents, a pixel **buffer** for collecting a complete row of an image's digital equivalent, a frame **buffer** for collecting all rows of an image's digital equivalent, and a selectively adjustable digital...

...that the digital image can be directly read into most word processing, desktop publishing, and **data base** software packages including means for executing the appropriate selected decompression algorithm; and a memory input/output interface that provides both **temporary storage** of the digital image and controls the transmission and interface with a standard Personal Computer...

...D) converter circuit to convert the analog picture signals into their digital equivalents, a pixel **buffer** for collecting a complete row of an image's digital equivalent, a frame **buffer** for collecting all rows of an image's digital equivalent, and a selectively adjustable digital...

...that the digital image can be directly read into most word processing, desktop publishing, and **data base** software packages including means for executing the appropriate selected decompression algorithm; and a memory input/output interface that provides both **temporary storage** of the digital image and controls the transmission and interface with a standard Personal Computer...

...D) converter circuit to convert the analog picture signals into their digital equivalents, a pixel **buffer** for collecting a complete row of an image's digital equivalent, a frame **buffer** for collecting all rows of an image's digital equivalent, and a selectively adjustable digital...

...that the digital image can be directly read into most word processing,

desktop publishing, and **data base** software packages including means for executing the appropriate selected decompression algorithm; and a memory input/output interface that provides both **temporary storage** of the digital image and controls the transmission and interface with a standard Personal Computer...

...D) converter circuit to convert the analog picture signals into their digital equivalents, a pixel **buffer** for collecting a complete row of an image's digital equivalent, a frame **buffer** for collecting all rows of an image's digital equivalent, and a selectively adjustable digital...

...that the digital image can be directly read into most word processing, desktop publishing, and **data base** software packages including means for executing the appropriate selected decompression algorithm; and a memory input/output interface that provides both **temporary storage** of the digital image and controls the transmission and interface with a standard Personal Computer...

...converter circuit (8) to convert the analog picture signals into their digital equivalents, a pixel **buffer** (10) for collecting a complete row of an image's digital equivalent, a frame **buffer** (11) for collecting all rows of an image's digital equivalent,and a selectively adjustable...
...that the digital image can be directly read into most word processing, desktop publishing, and **data base** software packages.
Claims:
...A **digital data compression** algorithm is applied to the digital signals to generate compressed information signals. There are operator selectable controls for controlling **digital data** format compatibility between the **compressed** signals, and one of a number of operator selectable types of computer apparatus...

...by different computers;</br> arranging the digital image data in accordance with said selected distinct output **data file** format; and</br> storing the thus arranged computer compatible digital image data in a digital memory...

...corresponding to a subject image,</br>means for converting said analog signals into corresponding digital data,</br> **buffer** storage means for accumulating a complete image frame of said digital data,</br>memory means for storing an output **data file** format determining code data,</br>output **data file** format determining means for retrieving said previously stored output **data file** format code data corresponding to one of a plurality of different input data formats for different formats for different types of information handling apparatus,</br>logic means responsive to said output **data file** format determining means for selectively arranging said digital data and said output format code data into a predetermined formatted output **data file** wherein said predetermined formatted output **data file** corresponds in file structure and arrangement to the input **data file** format of a predetermined type of data processing apparatus,</br>memory formatting control means for checking...

...status of a removably mounted digital memory means to ensure correspondence with said stored output **data file** format determining code data, and</br>means for removably mounting said digital memory means for storing...

15/69,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0010502733 - Drawing available
WPI ACC NO: 2001-103799/200112
XRPX Acc No: N2001-076846
Method for adhering to coherence protocol for data storage **system especially computer** cache , **includes switching of first status of entry in first** cache **through first** cache **into second status, so that entry of first** cache **can be cleared**
Patent Assignee: HEWLETT-PACKARD CO (HEWP)
Inventor: BRAIN; GAITHER B D; RENTSCHLER E M
Patent Family (4 patents, 3 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	
DE 10006430	A1	20001026	DE 10006430	A	20000214	200112	B
JP 2000322318	A	20001124	JP 2000112465	A	20000413	200112	E
US 6360301	B1	20020319	US 1999290430	A	19990413	200224	E
DE 10006430	B4	20041118	DE 10006430	A	20000214	200475	E

Priority Applications (no., kind, date): DE 10006430 A 20000214; US 1999290430 A 19990413

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
DE 10006430	A1	DE	10	6	
JP 2000322318	A	JA	6		

Alerting Abstract DE A1

NOVELTY - The method comprises inputting by means of a first **cache** (316) that an entry was cleared by a **cache** of a higher plane (304-308); and switching of a first status (406,504,602) of the entry in the first **cache** through the first **cache** in a second status (408,508,608), so that the entry of the first **cache** can be cleared without his having to be cancelled in the **cache** of a higher plane.

USE - In multiprocessor computer systems which use **cache** memories, and in particular to coherence protocol.

ADVANTAGE - Makes possible **improved behavior** of the **cache** memory.

DESCRIPTION OF DRAWINGS - The drawing shows a block diagram of an example of a computer system suitable for use with the method.

304-308 Higher plane **cache**
316 First **cache**
406,504,602 First status
408,508,608 Second status

Title Terms/Index Terms/Additional Words: METHOD; ADHERE; COHERE; PROTOCOL; DATA; STORAGE; SYSTEM; COMPUTER; **CACHE** ; SWITCH; FIRST; STATUS; ENTER; THROUGH; SECOND; SO; CAN; CLEAR

Class Codes
International Classification (Main): G06F-012/08, G06F-012/12
(Additional/Secondary): G06F-015/16, G06F-015/177
US Classification, Issued: 711143000, 711141000, 711142000, 711144000, 711145000, 711146000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F02C; T01-H03A

Method for adhering to coherence protocol for data storage **system** especially computer cache , **includes switching of first status of entry in first** cache **through first** cache **into second status, so that entry of first** cache **can be cleared**

Original Titles:
Verbessertes Koharenzprotokoll fur einen Computer- **Cache**
...
...COHERENCY PROTOCOL FOR COMPUTER **CACHE**
...

...Coherency protocol for computer **cache** .

Alerting Abstract ...NOVELTY - The method comprises inputting by means of a first **cache** (316) that an entry was cleared by a **cache** of a higher plane (304-308); and switching of a first status (406,504,602) of the entry in the first **cache** through the first **cache** in a second status (408,508,608), so that the entry of the first **cache** can be cleared without his having to be cancelled in the **cache** of a higher plane.USE - In multiprocessor computer systems which use **cache** memories, and in particular to coherence protocol...

...ADVANTAGE - Makes possible **improved behavior** of the **cache** memory
...

...304-308 Higher plane **cache**
...

...316 First **cache**

Title Terms.../Index Terms/Additional Words: **CACHE** ;

Original Publication Data by Authority

Original Abstracts:
Ein Cache einer unteren Ebene **erfasst** , wenn eine Speicherzelle von einem Cache einer hoheren Ebene **geraumt** wurde. Das Cache-Koharenzprotokoll fur den **Cache** einer unteren Ebene **setzt** die Zeile in einen besonderen Zustand. Wird eine Zeile in dem besonderen Zustand von dem Cache einer unteren Ebene **geraumt** , weiss der Cache einer unteren Ebene, **dass** die Zeile nicht in einem Cache einer hoheren Ebene **gespeichert** ist, weshalb keine Zuruckungultigmachungs-Transaktion benotigt wird. Ein Reduzieren der Anzahl von Zuruckungultigmachungs-Transaktionen verbessert...

...A lower level cache detects when a line **of** memory has been evicted from a higher level cache. The cache coherency protocol **for** the **lower** level cache places the line into **a** special state. If a line in the special state is evicted from the lower level cache, the lower level cache **knows** that the line **is** not cached at a higher level, **and** therefore a back-invalidate transaction is not needed. Reducing the number **of back** -invalidate transactions **improves** the performance of the **system.**
Claims:
...einer Koharenz fur ein Datenspeichersystem, mit folgenden Schritten: Erfassen durch einen ersten Cache (316), dass **ein** Eintrag durch einen Cache einer hoheren Ebene (304- **308**) geraumt wurde; Schalten eines ersten Zustands (406, 504, 602) des Eintrags in dem ersten Cache durch den ersten Cache in einen zweiten Zustand (408, 508, 608), von dem **der** Eintrag von dem **ersten**

Cache geraumt werden kann, ohne dass er in dem Cache einer hoheren Ebene ungultig gemacht werden muss.

...

...Ebene (304-308) geraumt wurde, wobei der Eintrag vor der Raumung in einem "Exklusiv"-Zustand (**602**) war; und Schalten des "Exklusiv"-Zustandes (602) des **Eintrags** in dem ersten Cache (316) in einen "Exklusiv und Nicht-Cache-gespeichert"-Zustand (608...

.....cache, a first state of the entry in the first cache, to a second state **from** **which** the entry can be evicted from the first cache without having to be **invalidated** in the higher level cache, the second state being in **addition** to an Exclusive state.

```
Set     Items   Description
S1    1174516   DATABASE OR DATABANK OR DATA()(BASE? OR BANK? OR FILE? OR -
            REPOSITOR? OR WAREHOUSE? OR STORE? ? OR STORAG?) OR DB OR RDB
            OR OODB OR ODBC OR DBMS
S2     400388   (TEMPORAR? OR RAM OR VOLITIL?)(3N)(STORE? ? OR STORAG? OR -
            STORING) OR BUFFER? OR CACHE? ? OR CACHING
S3    1392241   (UPGRAD? OR REVIS? OR BETTER? OR ENHANC? OR IMPROV? OR AUG-
            MENT? RAIS??? OR INCREAS? OR BOOST?)(5N)(PERFORM? OR EXECUT? -
            OR FUNCTION? OR OPERAT? OR OPTIMI? OR HANDL? OR BEHAV? OR CAP-
            AB?)
S4      25851   (COMPRESS? OR REDUC? OR (CUT OR CUTS OR CUTT? OR DROP? OR -
            LEAV??? OR BOX??? OR RECTANG?)(2W)(OUT OR OFF? ?) OR DECREAS?
            OR DECREMENT? OR PARE? OR SHORTEN? OR PARS???)(7N)(BIT OR BITS
             OR BINARY()DIGIT? ? OR DIGITAL()DATA? ?)
S5       5693   (SHRINK? OR CURTAIL? OR LESSEN? OR LOWER? OR ABRIDG? OR DI-
            SCARD? OR EXCIS? OR DELET? OR RECTANG? OR (BOX OR BOXES OR BO-
            XED OR BOXING)()OUT)(5N)(BIT OR BITS OR BINARY()DIGIT? ? OR D-
            IGITAL()DATA? ?)
S6      48177   ((UN OR "NOT" OR IR OR IN)(2N)(RELEVAN? OR WANT??? ? OR NE-
            ED??? ? OR DESIR??? ? OR IMPORTAN?) OR UNDESIR? OR UNWANT? OR
            INSIGNIF? OR UNIMPORTAN?)(5N)(BIT OR BITS OR BINARY()DIGIT? ?
            OR DIGITAL()DATA? ? OR CONTENT? ? OR NUMBER? OR DIGIT? OR CHA-
            RACT?)
S7        839   S6(7N)(DELET? OR REMOV? OR ERADICAT? OR ELIMINAT? OR ERAS?-
            ?? OR EDIT??? OR EXTRACT? OR (CUT OR CUTS OR CUTT? OR DROP? OR
             LEAV??? OR BOX??? OR RECTANG?)(2W)(OUT OR OFF? ?))
S8       3117   S3 AND S2 AND S1
S9         16   S8 AND (S4:S5 OR S7)
S10        16   S8 AND S6
S11        16   S9 NOT S10
S12         0   S10 AND COMPRESS?
S13        12   S9 NOT (PY>2001 OR PY=2002:2007)
S14        10   RD  (unique items)
S15         9   S10 NOT (PY>2001 OR PY=2002:2007)
S16         3   RD  (unique items)
S17        10   S8 AND (QUANTIS? OR QUANTIZ)
S18        32   S9:S16
S19         8   S17 NOT S18
S20         7   RD  (unique items)
S21        44   S8 AND (QUANTIS? OR QUANTIZ?)
S22        34   S21 NOT S17
S23        14   S22 NOT (PY>2001 OR PY=2002:2007)
S24        12   RD  (unique items)
S25         9   S24 NOT S18
File   2:INSPEC 1898-2007/May W2
         (c) 2007 Institution of Electrical Engineers
File   6:NTIS 1964-2007/May W4
         (c) 2007 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1884-2007/May W2
         (c) 2007 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2007/May W4
         (c) 2007 The Thomson Corp
File  35:Dissertation Abs Online 1861-2007/May
         (c) 2007 ProQuest Info&Learning
File  56:Computer and Information Systems Abstracts 1966-2007/May
         (c) 2007 CSA.
File  60:ANTE: Abstracts in New Tech & Engineer 1966-2007/May
         (c) 2007 CSA.
File  62:SPIN(R) 1975-2007/May W1
         (c) 2007 American Institute of Physics
File  65:Inside Conferences 1993-2007/May 24
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File 95:TEME-Technology & Management 1989-2007/May W3

File 99:Wilson Appl. Sci & Tech Abs 1983-2007/Apr

File 111:TGG Natl.Newspaper Index(SM) 1979-2007/May 21

File 144:Pascal 1973-2007/May W2

File 239:Mathsci 1940-2007/Jun

File 256:TecInfoSource 82-2007/Jul

File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec

File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13

****Your Assignee****

14/7/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

07965773 INSPEC Abstract Number: C2001-08-6120-009
Title: Optimizing multidimensional index trees for main memory access
Author(s): Kihong Kim; Cha, S.K.; Kwon, K.
Author Affiliation: Sch. of Electr. Eng. & Comput. Sci., Seoul Nat. Univ., South Korea
Journal: SIGMOD Record Conference Title: SIGMOD Rec. (USA) vol.30, no.2 p.139-50
Publisher: ACM, bad date
Publication Date: June 2001 Country of Publication: USA
CODEN: SRECD8 ISSN: 0163-5808
SICI: 0163-5808(200106)30:2L.139:OMIT;1-T
Material Identity Number: A660-2001-003
Conference Title: 2001 ACM SIGMOD International Conference on Management of Data
Conference Date: 21-24 May 2001 Conference Location: Santa Barbara, CA, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Practical (P)
Abstract: Recent studies have shown that **cache** -conscious indexes such as the CSB+-tree outperform conventional main memory indexes such as the T-tree. The key idea of these **cache** -conscious indexes is to eliminate most of the child pointers from a node to increase the fanout of the tree. When the node size is chosen in the order of the **cache** block size, this pointer elimination effectively reduces the tree height, and thus **improves** the **cache behavior** of the index. However, the pointer elimination cannot be directly applied to multidimensional index structures such as the R-tree, where the size of a key, typically an MBR (minimum bounding rectangle), is much larger than that of a pointer. Simple elimination of four-byte pointers does not help much to pack more entries in a node. The paper proposes a **cache** -conscious version of the R-tree called the CR-tree. To pack more entries in a node, the CR-tree compresses MBR keys, which occupy almost 80% of index data in the two-dimensional case. It first represents the coordinates of an MBR key relatively to the lower left corner of its parent MBR to eliminate the leading 0's from the relative coordinate representation. Then, it quantizes the relative coordinates with a fixed number of **bits** to further **cut off** the trailing less significant **bits** . Consequently, the CR-tree becomes significantly wider and smaller than the ordinary R-tree. Our experimental and analytical study shows that the two-dimensional CR-tree performs search up to 2.5 times faster than the ordinary R-tree while maintaining similar update performance and consuming about 60% less memory space. (20 Refs)
Subfile: C

14/7/6 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

09107746 Genuine Article#: 367MA Number of References: 16
Title: Adaptive vector quantisation for electrocardiogram signal compression using overlapped and linearly shifted codevectors
Author(s): Miaou SG (REPRINT) ; Larn JH
Corporate Source: CHUNG YUAN CHRISTIAN UNIV,DEPT ELECT ENGN, COMMUN TECHNOL RES LAB/CHUNGLI//TAIWAN/ (REPRINT)
Journal: MEDICAL & BIOLOGICAL ENGINEERING & COMPUTING, 2000, V38, N5 (SEP) , P547-552
ISSN: 0140-0118 Publication date: 20000900
Publisher: PETER PEREGRINUS LTD, MICHAEL FARADAY HOUSE, SIX HILLS WAY, STEVANAGE, HERTS SG1 2AY, ENGLAND
Language: English Document Type: ARTICLE
Abstract: A discrete semi-periodic signal can be described as x(n) = x(n + T + DeltaT) + Deltax,For Alln, where T is the fundamental period, DeltaT represents a random period variation, and Deltax is an amplitude variation. Discrete ECG signals are treated as semi-periodic, where T and Deltax are associated with the heart beat rate and the baseline drift, respectively. These two factors cause coding inefficiency for ECG signal compression using vector quantisation (VQ). First, the periodic characteristic of ECG signals creates data redundancy among codevectors in a traditional two-dimensional codebook. Secondly, the fixed codevectors in traditional VQ result in low adaptability to signal variations. To solve these two problems simultaneously, an adaptive VQ (AVQ) scheme is proposed, based on a one-dimensional (1D) codebook structure, where codevectors are overlapped and linearly shifted. To further **enhance** the coding **performance** , the dr term is extracted and encoded separately before 1D-AVQ is applied. The data in the first 3 min of all 48 ECG records from the MIT/BIH arrhythmic **database** are used as the test signals, and no codebook training is carried out in advance. The **compressed** data rate is 265.2 +/- 92.3 **bits** s(-1) at 10.0 +/- 4.1% PRD. No codebook storage or transmission is required. Only a very small codebook **storage** space is needed **temporarily** during the coding process. In addition, the linearly shifted nature of codevectors makes this easier to be hardware implemented than any existing AVQ method.

25/7/7 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01749479 ORDER NO: AADAA-I0801581
Video compression with complete information for pre-recorded sources
Author: Baylon, David Michael
Degree: Ph.D.
Year: 2000
Corporate Source/Institution: Massachusetts Institute of Technology (0753)
Supervisor: Jae S. Lim
Source: VOLUME 61/06-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 3192.

Traditional video compression algorithms focus on causal processing of the video data. The causal constraint is necessary for real-time video programs where delay is an important consideration. However, many video programs such as movies are pre-recorded and can be processed offline prior to compression. This thesis proposes using pre-processing for pre-recorded video programs to obtain useful information for compression. By exploiting information obtained about a program prior to compression, better video quality can be achieved. In particular, as an example of how complete noncausal knowledge of a video program can be used to **improve performance** over causal knowledge, a new iterative algorithm is developed for a **buffer** -constrained **quantization** problem to reduce the number of **quantization** changes in MPEG-2 intraframe video compression. This algorithm is shown to be optimal under certain conditions. By introducing a noncausally computed parameter into the distortion **function** , experiments have shown that **improved** and more constant video quality can be delivered using the noncausal approach relative to a traditional causal approach. Gains of up to 1.0 **dB** in PSNR were observed in multiscene sequences, corresponding to savings of up to 10% in bit rate. (Copies available exclusively from MIT Libraries, Rm. 14-0551, Cambridge, MA 02139-4307. Ph. 617-253-5668; Fax 617-253-1690.)

25/7/8 (Item 2 from file: 35)

01461212 ORDER NO: AADAA-INN99725

DECODAGE SIMPLIFIE: ALGORITHME ADAPTATIF POUR CODES CONVOLUTIONNELS ET TECHNIQUE DE PERFORATION POUR MODULATION CODEE (CONVOLUTIONAL CODES, VITERBI ALGORITHM, TRELLIS CODED MODULATION, DECODING, FRENCH TEXT)

Author: CHAN, FRANCOIS
Degree: PH.D.
Year: 1994
Corporate Source/Institution: UNIVERSITE DE MONTREAL (CANADA) (0992)
Directeur: D. HACCOUN
Source: VOLUME 56/10-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 5665. 224 PAGES
Language: FRENCH
ISBN: 0-315-99725-7

A widely used decoding algorithm for convolutional codes, the Viterbi Algorithm (VA), requires a computational effort which increases exponentially with the constraint length K of the code, limiting it in practice to $K\le9$. Furthermore, for convolutional codes or Trellis-Coded Modulation (TCM) codes with a rate $R=b/V$, decoding complexity also grows exponentially with b. The objective of this research is to simplify the decoding of both convolutional codes and TCM codes.

The Adaptive Viterbi Algorithm (AVA), which provides over a Binary Symmetric Channel an error performance very close to that of the VA at a reduced average complexity, defined as the number of survivors, is modified to accept 3-bit soft- **quantization** of the channel output. Computer simulations show that over an Additive White Gaussian Noise (AWGN) channel, a gain exceeding 2 **dB** is obtained compared to hard- **quantization** with hardly any increase of the complexity. Compared to the VA with a K = 7 code, codes with a constraint length K up to 11 can be used with the AVA to achieve an **improved** bit error **performance** while maintaining a similar average complexity and requiring only an input **buffer** of modest size.

The performance of the AVA over a mobile radio channel with Rayleigh fading is also investigated. As in the AWGN channel case, for a given code, the AVA yields almost the same error performance as the VA while reducing substantially the average decoding complexity. With a normalized fading rate F$\sb{\rm D}$T = 0.1, the AVA using a more powerful code offers approximately a gain of 2 **dB** over the VA with K = 7 without increasing the average complexity.

For TCM codes, the technique of punctured convolutional coding is used to simplify decoding. This technique, which is widely used for convolutional codes of rate $R=b/V$, allows a reduction of the number of binary comparisons required at each state of the trellis from ($2\sp{b}-1$) to b. An extensive computer search for the best punctured TCM codes has provided new codes for QPSK, 8-PSK, 16-PSK and 16-QAM modulation schemes. The performance of these codes is analyzed and compared to the best known TCM codes, discovered by Ungerboeck.

With usual decoding, requiring ($2\sp{b}-1$) comparisons per state, simulations have confirmed that the error performance of these codes is similar to that of the best known codes. Using the technique of punctured coding, two simplified decoding methods, called approximate decoding and staged decoding, have been investigated. Simplified decoding leads to a slight degradation of the performance, but the degradation is modest (0.15 **dB** for the 64-state 8-PSK code at P(B) = 10$\sp{-4}$). The decoding complexity reduction is the same as with binary convolutional codes, that is, 2 comparisons per state instead of 3, for 8-PSK codes. (Abstract shortened by UMI.)

```
Set     Items   Description
S1     319430   DATABASE OR DATABANK OR DATA()(BASE? OR BANK? OR FILE? OR -
             REPOSITOR? OR WAREHOUSE? OR STORE? ? OR STORAG?) OR DB OR RDB
             OR OODB OR ODBC OR DBMS
S2     411218   (TEMPORAR? OR RAM OR VOLITIL?)(3N)(STORE? ? OR STORAG? OR -
             STORING) OR BUFFER? OR CACHE? ? OR CACHING
S3     435369   (UPGRAD? OR REVIS? OR BETTER? OR ENHANC? OR IMPROV? OR AUG-
             MENT? RAIS??? OR INCREAS? OR BOOST?)(5N)(PERFORM? OR EXECUT? -
             OR FUNCTION? OR OPERAT? OR OPTIMI? OR HANDL? OR BEHAV? OR CAP-
             AB?)
S4      30608   (COMPRESS? OR REDUC? OR (CUT OR CUTS OR CUTT? OR DROP? OR -
             LEAV??? OR BOX??? OR RECTANG?)(2W)(OUT OR OFF? ?) OR DECREAS?
             OR DECREMENT? OR PARE? OR SHORTEN? OR PARS???)(7N)(BIT OR BITS
              OR BINARY()DIGIT? ? OR DIGITAL()DATA? ?)
S5      19356   (SHRINK? OR CURTAIL? OR LESSEN? OR LOWER? OR ABRIDG? OR DI-
             SCARD? OR EXCIS? OR DELET? OR RECTANG? OR (BOX OR BOXES OR BO-
             XED OR BOXING)()OUT)(5N)(BIT OR BITS OR BINARY()DIGIT? ? OR D-
             IGITAL()DATA? ?)
S6      69606   ((UN OR "NOT" OR IR OR IN)(2N)(RELEVAN? OR WANT??? ? OR NE-
             ED??? ? OR DESIR??? ? OR IMPORTAN?) OR UNDESIR? OR UNWANT? OR
             INSIGNIF? OR UNIMPORTAN?)(5N)(BIT OR BITS OR BINARY()DIGIT? ?
             OR DIGITAL()DATA? ? OR CONTENT? ? OR NUMBER? OR DIGIT? OR CHA-
             RACT?)
S7       2488   S6(7N)(DELET? OR REMOV? OR ERADICAT? OR EDIT??? OR ELIMINA-
             T? OR ERAS??? OR EXTRACT? OR (CUT OR CUTS OR CUTT? OR DROP? OR
              LEAV??? OR BOX??? OR RECTANG?)(2W)(OUT OR OFF? ?) OR QUANTIS?
              OR QUANTIZ?)
S8       2933   S1(100N)S2(100N)S3
S9         56   S8(100N)(S4:S5 OR S7)
S10        32   S9 NOT (AD>2001 OR AD=2002:2007)
S11        38   S8(100N)(QUANTIS? OR QUANTIZ?)
S12         1   S11(100N)S6
S13        52   S8(100N)S6
S14         1   S13(100N)(QUANTIS? OR QUANTIZ?)
S15         0   S14 NOT S12
File 348:EUROPEAN PATENTS 1978-2007/ 200720
         (c) 2007 European Patent Office
File 349:PCT FULLTEXT 1979-2007/UB=20070518UT=20070510
         (c) 2007 WIPO/Thomson
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12/5,K/1 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00937157 **Image available**
COMPRESSION SCHEME FOR IMPROVING CACHE BEHAVIOR IN DATABASE SYSTEMS
PROGRAMME DE COMPRESSION PERMETTANT D'AMELIORER LE COMPORTEMENT DU CACHE DANS LES SYSTEMES DE BASES DE DONNEES

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AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
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Claims
Fulltext Word Count: 11152

English Abstract
A cache-conscious version of the R-tree, called the CR-tree, is disclosed. To pack more entries in a node, the CR-tree compresses MBR keys, which occupy substantial part of the index data. It first represents the coordinates of an MBR key relatively to the lower left corner of its parent MBR to eliminate the leading 0's from the relative coordinate representation. Then, it quantizes the relative coordinates with a fixed number of bits to further cut off the trailing less significant bits. Consequently, the CR-tree becomes significantly wider and smaller than the ordinary R-tree. The experimental and analytical results show that the two-dimensional CR-tree performs search faster than the ordinary R-tree while maintaining similar update performance and consuming less memory space.

French Abstract
L'invention porte sur une version consciente de cache de l'arbre R

appelee arbre CR. Afin de regrouper davantage d'entrees dans un noeud, l'arbre CR comprime les cles MBR qui occupent une partie substantielle des donnees d'index. Cet arbre represente d'abord les coordonnees d'une cle MBR par rapport au coin gauche inferieur de son ascendant MBR afin d'eliminer les 0 superieurs de la representation de coordonnees relatives. Il quantifie ensuite les coordonnees relatives au moyen d'un chiffre fixe de bits afin de supprimer, par la suite, les bits arriere les moins signifiants. Par consequent, l'arbre CR gagne sensiblement en largeur et devient nettement plus petit que l'arbre R habituel. Les resultats experimentaux et analytiques montrent que l'arbre CR bi-dimensionnel effectue des recherches de maniere plus rapide que l'arbre R habituel tout en conservant la meme qualite de mise a jour et en prenant moins d'espace memoire.

Legal Status (Type, Date, Text)
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Fulltext Availability:
Detailed Description
Claims

Detailed Description
... as the R-tree, which have numerous application 2o domains such as spatio-temporal databases, **data warehouses** , and directory servers.

The data object stored in an R-tree are approximated by, so...

...is not big enough to make any significant difference in the tree height for the **improved cache behavior** .
Therefore, there is a need for a scheme for **improving cache behavior** to in accessing multidimensional indexes to access main-memory **database** .

DISCLOSURE OF THE INVENTION
Recognizing that the MBR keys occupy most of index data in the multidimensional index, Ri-trees, the present invention achieves inexpensive
compression of MBR keys to **improve** the index **cache behavior** . A preferred
embodiment of the present invention, called "CR-Tree" (Cache -conscious R-Tree), where the child nodes are grouped into a parent node so that...

...further reduce the number of bits per MBR, the--CR-tree also cuts off trailing **insignificant bits** by **quantization** .

The analytical results and the experimental results agree showing that the compression technique can reduce...Figures 14A, 14B and 14C are graphs showing the ratio of false hits incurred by **quantization** .

Figures 15A and 15B are graphs showing the increase of MBR size with varying **quantization** levels.

Figures 16A, 16B and 16C are graphs showing the search time with varying **quantization** levels.

Figures 17A and 17B are graphs showing the amount of accessed index data.

Figures 18A and 18B are graphs showing the number of L2 **cache** misses.

Figures 19A and 19B are graphs showing the number of key comparisons.

Figures 20A...

...FOR CARRYING OUT THE INVENTION
The present invention is based on making the R-tree **cache** -conscious by compressing MBRs. An R-Tree is a height-balanced tree structure designed specifically for indexing multi-dimensional data objects in a **database** . It stores the minimum bounding rectangle ("MBR!') with 2 or higher dimension of...

...present invention is also applicable to a variant of R-Tree called R*-Tree which **improves** the search **performance** by using a **better** heuristic for redistributing entries and dynamically reorganizing the tree during insertion. Those skilled in the...

...number of significant bits than absolute coordinates. FIG. IC shows the coordinates of Rl-R3 **quantized** into 16 levels or four **bits** by cutting off trailing **insignificant bits** . The resultant MBR is called **quantized** MBR ("QRMBW'). Note that QRMBRs can be slightly larger than original MBRs.

A preferred embodiment of the present invention is an index tree, called CRtree (" **cache** -conscious R-tree"), a R-tree variant that uses QRMBRs as index keys.

The number of **quantization** levels may be the same for all the nodes in a CR-tree.

FIG. 2A...

Claim
1 A method of **improving** the **cache behavior** of accessing a multidimensional index structure resident in main memory for facilitating reference to data objects stored in a **database** , where the index structure consists of internal nodes having pointers to child nodes and leaf nodes having to **database** objects, the method comprising the steps of:
associating with each node a minimum bounding rectangle...

...represented relative to the coordinates of
a reference MBR; and
compressing each RMBRs into a **quantized** , RMBR ("QRMBR") by quantizing each RMBR to finite precision by cutting off trailing **insignificant bits** after quantization.

2 The method of claim 1, wherein said multi-dimensional index structure is...

...QRMBRs while the leaf nodes store NMRs.

10 The method of claim 1, wherein said **database** resides in main memory.
1 5 11. The method of claim 1, wherein said **database** resides in disk.

12 A method of **improving** the **cache behavior** of accessing a multidimensional index structure resident in main memory for facilitating reference to data objects stored in a **database** , where the index structure consists of internal nodes having pointers to child nodes and leaf nodes having to **database** objects, the method comprising the steps of. associating with each node a minimum bounding shape...

...the coordinates of a reference minimum bounding shape; and compressing each relative representation into a **quantized** representation by **quantizing** each relative representation to finite precision by cutting off trailing **insignificant bits** after quantization.

13 The method of claim 12, wherein each internal node has a plurality...
?